

In re application of

Keiichi MURAYAMA et al.

Confirmation No. 6969

Serial No. 10/748,158

[Group Art Unit 2826

Filed December 31, 2003

Examiner Tuan N. Quach]

HETERO-JUNCTION BIPOLAR TRANSISTOR
AND MANUFACTURING METHOD THEREOF Mail Stop ISSUE FEE

SUBMISSION OF FORMAL DRAWINGS

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

As required by the Examiner in the Notice of Allowability mailed February 3, 2005, 6 sheets of formal (A4 paper) drawings (Figs. 1-6C) are submitted herewith.

Respectfully submitted,

Keiichi MURAYAMA et al.

By:

Michael S. Huppert Registration No. 40,268 Attorney for Applicants

MSH/kjf

Washington, D.C. 20006-1021 Telephone: (202) 721-8200 Facsimile: (202) 721-8250

April 7, 2005

THE COMMISSIONER IS AUTHORIZED TO CHARGE ANY DEFICIENCY IN THE FEES FOR THIS PAPER TO DEPOSIT ACCOUNT NO. 23-0975